An efficient power supply for the Contactless Energy Transfer Project

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Contents

Chapter 1

Introduction

In this chapter, first, an overview is given of what the complete project is about. After that, the internship problem description is presented.

1.1 Project overview

1.1.1 Involved people

The following people are involved with the project:

Name	Position
Christoph Sonntag	PhD Student
prof. dr. ir. J.H. Blom	First Promotor
dr. J.L. Duarte	Co-Promotor
ir. M.A.M. Hendrix	Co-Promotor
dr. E. Lomonova, M.Sc.	Co-Promotor
M.A. Koch, B. Eng.	Student on work placement

1.1.2 Topic

Contactless energy transfer for domestic and office applications.

1.1.3 Introduction

Contactless Energy Transfer (CET) is the process in which electrical energy is transferred between primary and secondary coils through inductive coupling across a gap without the use of a conventional core-based transformer core.

1.1.4 Objective

The objective of this project is to develop and demonstrate techniques by which power is transmitted between electronic devices without the use of naked contacts or "plug-and-socket" mechanisms but by inductive energy transfer, even if there is relative motion.

The potential applications for such a technology are practically endless and can range from the transfer of energy between low power home and office devices to high powered industrial applications.

Medical, marine, and other applications where physical electrical contact might be dangerous, impossible or at the very least problematic, are all prospective candidates for the use of contactless energy transfer.

The main application around which the initial research and development is concentrated is an application where flat planar CET coils are embedded into a desktop table for the purpose of powering and recharging electrical devices placed on the table, such as laptops, cellular phones, keyboards, mice, and screens.

The purpose of this project is not to develop one single application, but rather to create a set of tools (mathematical formula's, algorithms, computer programs, etc) and a development process ("instruction manual") which could be used to develop basically any CET system.

1.2 Internship problem description

1.2.1 Involved people

The following people are involved with the internship problem:

Name	Position
Christoph Sonntag	PhD Student
dr. J.L. Duarte	Assistant Professor
ir. M.A.M. Hendrix	Associate Professor
M.A. Koch, B. Eng.	Student on work placement

1.2.2 Topic

The design of a power supply for the Contactless Energy Transfer Project.

1.2.3 Introduction

For the Contactless Energy Transfer Project, an efficient switched power supply is needed to drive the CET coils with a square-wave output voltage form. Due to this waveform and the behavior of the coils, the output current will be *sinusoidal*.

1.2.4 Objective

The objective of this project is to design and simulate a single phase half-bridge switched power supply for driving a series of CET coils. The power supply will act like a current source and the switching frequency $f_s = \frac{1}{T_s}$ of the output voltage waveform equals 2.78 MHz.

The CET system operates in resonance, with the CET coils acting as band-pass filters for the current. The power supply will generate a square-wave voltage for driving the coils, of which the voltage amplitude will be controlled to maintain a 1.32 A sinusoidal rms current in the circuit with a frequency equal to the fundamental component of the square-wave output voltage. For this a controller is needed.

The CET coils have a maximum voltage drop of approximately 0.5 V when they are not transferring energy, and a maximum voltage drop of 10 V while transferring energy. The power supply is capable of driving at least 6 CET coils, so the maximum power supply output voltage equals at least 60 V at about 100 Watts.

Since the transfer of energy from the coils could be sharply interrupted, this can lead to a sudden drop in the voltage-drop of the individual coils. The controller is able to compensate for the increase in the primary current very fast, as not to cause an over voltage problem in the secondary coils.

The current in the primary circuit is adjustable and the power supply switching rate is driven by an external clock signal.

Figure 1.1 shows a block diagram of the power supply.

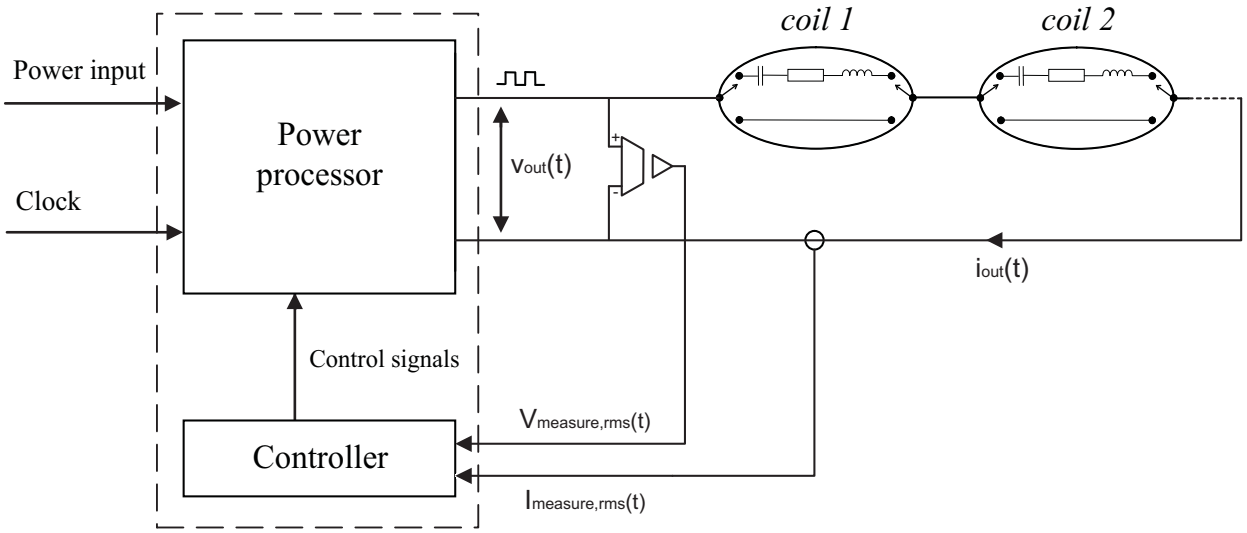


Figure 1.1: Block diagram of the power supply to be designed

Chapter 2

Theory

2.1 Introduction

This chapter deals with the theoretical part of the internship problem.

Throughout this chapter, for instantaneous values of variables such as voltage and current that are functions of time, the symbols used are lowercase letters v and i, respectively. The uppercase symbols V and I refer to root-mean-square (rms) values in ac quantities, and to average values in dc quantities. Bold letters like $\mathbf{V}$ and $\mathbf{I}$ are used to denote vectors.

2.2 CET coil

2.2.1 Introduction

The CET coil can be represented as a series connection of a capacitor, a resistor and an inductor. See figure 2.1.

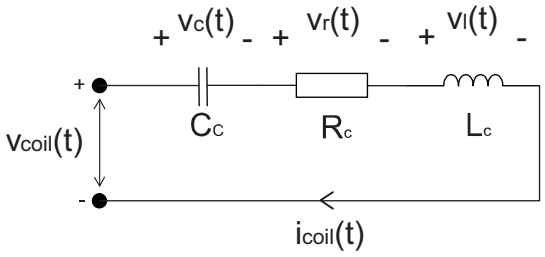


Figure 2.1: Representation of the coil as a series resonance circuit

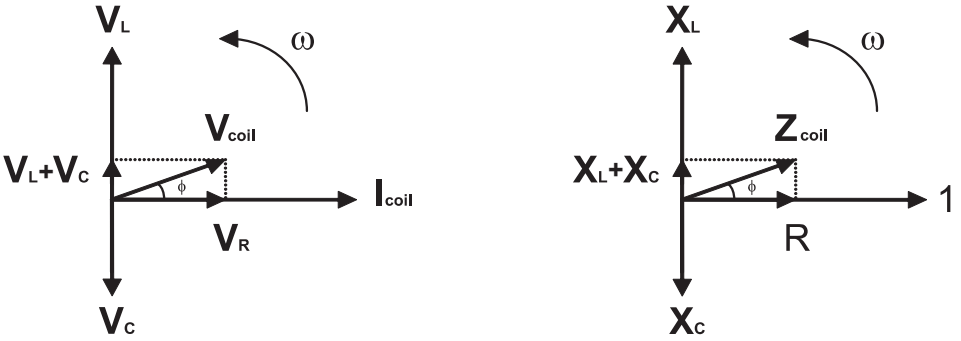
In the following, the subscript c (coil) of L, C and R is omitted for simplicity.

The coil acts as a series resonance circuit with a total impedance of

$$\begin{aligned} \mathbf{Z_{coil}} &= -jX_C + R + jX_L \\ &= R + j(\omega L - \frac{1}{\omega C}). \end{aligned} \tag{2.1}$$

2.2.2 Analysis single coil

The current which is flowing through L, C and R is the same. With this and (2.1) in mind, a phasor diagram can be made; see figure 2.2a. Because $\mathbf{I_{coil}}$ is drawn as being a real vector, we may divide all phasors by $|\mathbf{I_{coil}}|$ to obtain the impedance diagram of figure 2.2b. The phasors are rotating counterclockwise with angle speed ω.



(a) Phasor diagram (b) Impedance diagram

Figure 2.2: Vector diagrams of the series resonance circuit

Notice that the absolute values of the rms voltages across the inductor and the capacitor (i.e. $|\mathbf{V_L}|$ and $|\mathbf{V_C}|$, respectively) can be much higher than the absolute value of the supply voltage $|\mathbf{V_{coil}}|$ if R is small compared to X_L and X_C.

The circuit is in resonance if inductive reactance X_L equals capacitive reactance X_C, so if

$$\omega_{res}L = \frac{1}{\omega_{res}C} \;\Leftrightarrow\; \omega_{res} = \frac{1}{\sqrt{LC}}, \tag{2.2}$$

and this is similar to

$$f_{res} = \frac{\omega_{res}}{2\pi} = \frac{1}{2\pi\sqrt{LC}}. \tag{2.3}$$

With (2.3), the LC product can be calculated to be

$$LC = \frac{1}{4\pi^2 f_{res}^2}. \tag{2.4}$$

So for f_{res}=2.78 MHz, the LC product can now be calculated to be

$$LC \approx 3.278 \cdot 10^{-15}\ [HenryFarads]. \tag{2.5}$$

At the resonance frequency, from (2.1) and (2.2), the total impedance becomes

$$\mathbf{Z_{coil,res}} = R, \tag{2.6}$$

as can be seen from figure 2.2b. The phase difference at the resonance frequency between the output voltage and the output current can be calculated to be

$$\begin{aligned} \phi_{1,res} &= \arctan\left(\frac{\Im\{\mathbf{Z_{coil,res}}\}}{\Re\{\mathbf{Z_{coil,res}}\}}\right) \\ &= \arctan\left(\frac{0}{R}\right) \\ &= 0. \end{aligned} \tag{2.7}$$

This can also be seen by observing figure 2.2b.

If the coil is not in resonance , in the first case, if $\omega < \omega_{res}$ then in (2.1),

$$\omega L < \frac{1}{\omega C} \Leftrightarrow \omega L - \frac{1}{\omega C} < 0, \tag{2.8}$$

so we can say that for this frequency range the coil acts as a **capacitive** load, with the applied voltage lagging the current.

For the second case, if $\omega > \omega_{res}$, we can state that

$$\omega L > \frac{1}{\omega C} \Leftrightarrow \omega L - \frac{1}{\omega C} > 0, \tag{2.9}$$

so for this frequency range the coil acts as an **inductive** load, with the applied voltage leading the current.

In both situations there will be a nonzero phase shift between the voltage and the current of

$$\begin{aligned} \phi_1 &= \arctan\left(\frac{\omega L - \frac{1}{\omega C}}{R}\right) \\ &= \arctan\left(\frac{\omega^2 LC - 1}{\omega RC}\right). \end{aligned} \tag{2.10}$$

As an example, see figure 2.3 for the frequency response of a CET coil with a resonance frequency of 2.78 MHz.

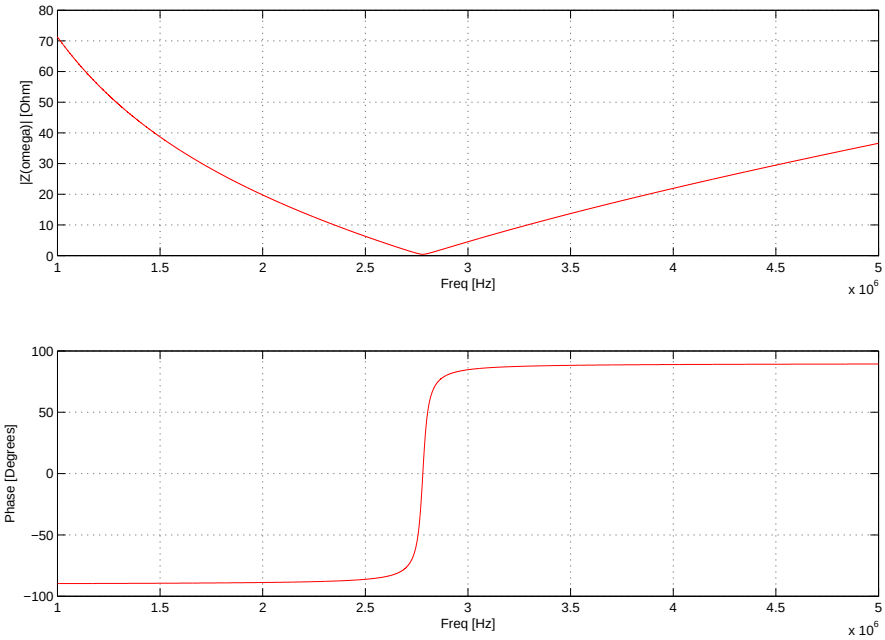


Figure 2.3: CET coil frequency response with R=0.4177 Ω, L=1.6866 μH and C=1.9433 nF

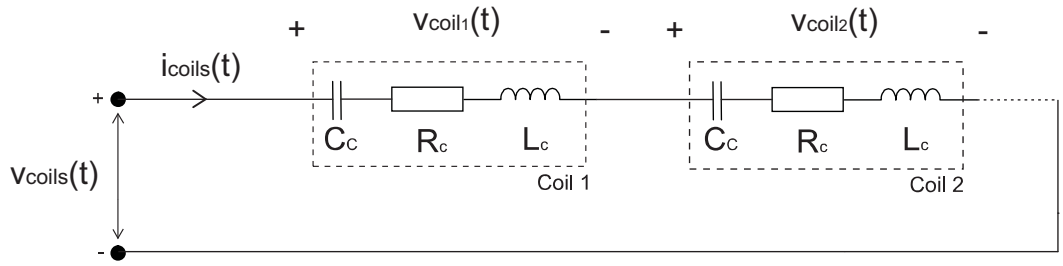


Figure 2.4: Multiple coils connected in series

2.2.3 Analysis multiple coils in series

Lateron, there could be a couple of coils connected to the output of the power supply as load, see figure 2.4.

If we assume the number of coils equals $n, \{n \in \mathbb{N} | n > 1\}$, the total impedance becomes

$$\begin{aligned} \mathbf{Z_{coils}} &= -jnX_C + (R_{C_1} + R_{C_2} + \ldots + R_{C_n}) + jnX_L \\ &= (R_{C_1} + R_{C_2} + \ldots + R_{C_n}) + jn\left(\omega L - \frac{1}{\omega C}\right) \end{aligned} \tag{2.11}$$

The circuit is in resonance if

$$X_L = X_C, \tag{2.12}$$

so (2.2)-(2.5) also hold here like the case of the single coil as load.

By (2.12), equation (2.11) implies that

$$\mathbf{Z_{coils,res}} = R_{C_1} + R_{C_2} + \ldots + R_{C_n}. \tag{2.13}$$

Because (2.13) doesn't have an imaginary part, the phase at the resonance frequency will be

$$\phi_{n,res} = \arctan(0) = 0. \tag{2.14}$$

Like in the single coil case, if $\omega < \omega_{res}$, the behavior of the series connection of the n coils is **capacitive**, and if $\omega > \omega_{res}$, this behavior is **inductive**.

When $\omega \neq \omega_{res}$, there will be a nonzero phase shift between the voltage and the current of

$$\phi_n = \arctan\left(\frac{n\left\{\omega L - \frac{1}{\omega C}\right\}}{R_{C_1} + R_{C_2} + \ldots + R_{C_n}}\right). \tag{2.15}$$

If we assume n equally loaded coils, the voltage across a single coil trivially equals

$$\mathbf{V_{coil_1}} = \mathbf{V_{coil_2}} = \ldots = \mathbf{V_{coil_n}} = \mathbf{V_{coil}} = \frac{\mathbf{V_{coils}}}{n}. \tag{2.16}$$

2.2.4 Practical CET coil

A practical CET coil consists of a spiroid hexagon PCB inductor in series with a capacitor to form the series resonance circuit. See figure 2.5 for an example picture of such a PCB inductor. The unloaded resistor value equals the total loss resistance of the circuit; there isn't explicitly placed one. By 'unloaded' the situation is meant where there is no inductive coupling with some other secondary coil, while 'maximum loaded' depicts the situation by which the maximum possible energy is inductively being transferred to a secondary coil.

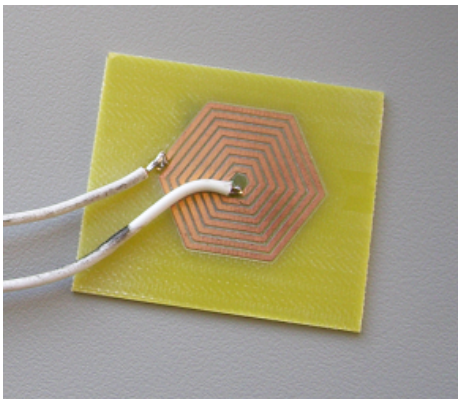


Figure 2.5: Example PCB inductor

After calculating, developing and measuring, Christoph came to the following 2.78 MHz resonant CET coil values which can be used (see figures 2.1 and 2.4):

$$\begin{aligned} L_C &= 1.6866\ \mu H \\ C_C &= 1.9433\ nF \\ R_C = [no\ load,\ max\ load] &= [0.4177, 8.4177]\ \Omega \end{aligned} \tag{2.17}$$

Remark that the loaded situation *increases* the resistor value (due to the inductive coupling with the secondary coils) and that (2.5) is satisfied.

2.3 Power supply output

2.3.1 Introduction

The power supply will generate a square-wave voltage with variable amplitude B[1] and has a fixed duty ratio of 0.5. Due to the characteristics of the load, the constant output current $\mathbf{I_{out}}$ will be sinusoidal at the resonance frequency.

2.3.2 Analysis

The instantaneous output voltage and current can be depicted as

$$v_{out}(t) = \begin{cases} B, & 0 < (t \bmod T_{res}) < \frac{T_{res}}{2} \\ -B, & \frac{T_{res}}{2} < (t \bmod T_{res}) < T_{res} \end{cases} \tag{2.18}$$

[1] B is used instead of A to prevent misunderstandings; A is also the unit of current, Ampère

$$i_{out}(t) = \sqrt{2}\,|\mathbf{I_{out}}|\,\sin(\omega_{res}t), \tag{2.19}$$

with ω_{res} being the frequency of resonance of the coil.

The general fourier series of the output voltage waveform repeating with angular frequency ω_{res} equals

$$v_{out}(t) = \frac{1}{2}a_0 + \sum_{h=1}^{\infty}\big\{a_h\cos(h\omega_{res}t) + b_h\sin(h\omega_{res}t)\big\}, \tag{2.20}$$

where $\frac{1}{2}a_0$ is the average value. In (2.20),

$$a_h = \frac{1}{\pi}\int_0^{2\pi} v_{out}(t)\cos(h\omega_{res}t)d(\omega_{res}t) \qquad h = 0,\ldots,\infty \tag{2.21}$$

$$b_h = \frac{1}{\pi}\int_0^{2\pi} v_{out}(t)\sin(h\omega_{res}t)d(\omega_{res}t) \qquad h = 1,\ldots,\infty. \tag{2.22}$$

Because (2.18) can also be expressed as

$$v_{out}(t) = \begin{cases} B, & 0 < \omega_{res}t < \pi \\ -B, & \pi < \omega_{res}t < 2\pi, \end{cases} \tag{2.23}$$

(2.21) becomes

$$a_h = \frac{B}{\pi}\left\{\int_0^{\pi}\cos(h\omega_{res}t)d(\omega_{res}t) - \int_{\pi}^{2\pi}\cos(h\omega_{res}t)d(\omega_{res}t)\right\}, \tag{2.24}$$

and this can be worked out to become

$$\begin{aligned} a_h &= \frac{B}{h\pi}\left\{\sin\ u\Big|_0^{h\pi} - \sin\ u\Big|_{h\pi}^{h2\pi}\right\} \\ &= \frac{B}{h\pi}\{0-0\} \\ &= 0\ \forall h. \end{aligned} \tag{2.25}$$

Similarly, (2.22) becomes

$$\begin{aligned} b_h &= \frac{B}{h\pi}\left\{(-\cos\ u)\Big|_0^{h\pi} + \cos\ u\Big|_{h\pi}^{h2\pi}\right\} \\ &= \frac{2B}{\pi h}\Big\{(-1)^{h-1}+1\Big\} \\ &= \frac{4B}{\pi h},\ \ h = odd. \end{aligned} \tag{2.26}$$

By (2.25) and (2.26), (2.20) becomes

$$\begin{aligned} v_{out}(t) &= \frac{4B}{\pi}\sum_{h=1,odd}^{\infty}\left\{\frac{\sin(h\omega_{res}t)}{h}\right\} \\ &= \frac{4B}{\pi}\Big\{\sin(\omega_{res}t) + \frac{\sin(3\omega_{res}t)}{3} + \frac{\sin(5\omega_{res}t)}{5} + \cdots\Big\}. \end{aligned} \tag{2.27}$$

The rms output voltage can be calculated with help of (2.18) as

$$\begin{aligned}\mathbf{V_{out}} &= \sqrt{\frac{1}{T_{res}}\int_0^{T_{res}} v_{out}^2(t)dt} \\ &= B\sqrt{\frac{1}{T_{res}}\int_0^{T_{res}} 1\cdot dt} \\ &= B\sqrt{\frac{1}{T_{res}}T_{res}} \\ &= B.\end{aligned} \tag{2.28}$$

From (2.27), there can be seen that the output voltage only contains fundamental frequency f_{res} and its odd upper harmonics $3f_{res}$, $5f_{res}$, and so on. Because the load, several CET coils, acts as a bandpass filter which suppresses all the upper harmonics, the only significant output current component will be the fundamental component with frequency f_{res}. All the upper harmonics of the output current are considerably suppressed, so they can be neglected.

The following presents a proof of this neglection. First, we identify the odd rms output voltage harmonic components from (2.27) as

$$\mathbf{V_{out_{h,odd}}} = \frac{4B}{h\pi\sqrt{2}}. \tag{2.29}$$

Now, assuming a n-coil load where every coil is equally loaded (we only bother about the minimum and maximum possible load anyway), the odd output current harmonic components can be written as

$$\begin{aligned}\mathbf{I_{out_{h,odd}}} &= \frac{\mathbf{V_{out_{h,odd}}}}{n\mathbf{Z_{coil_{\omega=h\omega_{res}}}}} \\ &= \frac{4B}{nh\pi\sqrt{2}}\cdot\frac{1}{R+j\left(h\omega_{res}L-\frac{1}{h\omega_{res}C}\right)}.\end{aligned} \tag{2.30}$$

Notice that if h increases, $\mathbf{I_{out_{h,odd}}}$ decreases, so the higher the harmonic component, the more it will be suppressed. Therefore, to proof of the neglection of the upper harmonics of the output current, it will be sufficient to proof that the 3rd harmonic is enough suppressed from the fundamental one.

By using a simple MATLAB script, the following unloaded and maximum loaded harmonic component values are calculated, by making use of the coil values of (2.17):

$$\begin{aligned}\mathbf{I_{out,noload_1}} &\approx 2.16\left(\frac{B}{n}\right)A\angle 0\,^\circ, \\ \mathbf{I_{out,noload_3}} &\approx 3.82\cdot 10^{-3}\left(\frac{B}{n}\right)A\angle -89.7\,^\circ, \\ \mathbf{I_{out,maxload_1}} &\approx 106.96\cdot 10^{-3}\left(\frac{B}{n}\right)A\angle 0\,^\circ, \\ \mathbf{I_{out,maxload_3}} &\approx 3.80\cdot 10^{-3}\left(\frac{B}{n}\right)A\angle -83.9\,^\circ.\end{aligned} \tag{2.31}$$

So the 3rd harmonic, compared to the fundamental one, is suppressed within a range of

$$S_{3,dB} = -20\log_{10}\left(\frac{|\,\mathbf{I_{out_3}}\,|}{|\,\mathbf{I_{out_1}}\,|}\right) = [29.0, 55.0]\ dB, \tag{2.32}$$

when the load is decreased from the maximum value to 0. Note the independency of B and n.

With a minimum harmonic suppression of 29 dB, we can state that the influence of this harmonics to the output current is neglectible. Hence the output current is real and equals

$$I_{out} = \mathbf{I_{out}} \approx \mathbf{I_{out_1}}, \tag{2.33}$$

so the output voltage amplitude B can be calculated to become

$$B \approx \frac{\pi \left(R_{C_1} + R_{C_2} + \ldots + R_{C_n}\right)}{\sqrt{8}} I_{out}. \tag{2.34}$$

Because the CET coils act as band-pass filters, only the fundamental components of the output voltage and the output current are contributing for the output power. Hereby, the complex output power with n CET coils as load equals

$$\begin{aligned} \mathbf{S_{out}} &= \mathbf{V_{out_1}} \mathbf{I^*_{out_1}} \\ &= \frac{\sqrt{8}B}{\pi} I_{out} \\ &\approx I^2_{out} \left(R_{C_1} + R_{C_2} + \ldots + R_{C_n}\right), \end{aligned} \tag{2.35}$$

and because there is no imaginary part, this power is real:

$$\mathbf{S_{out}} = P_{out} + jQ_{out} = P_{out} \;\Leftrightarrow\; P_{out} = \mathbf{S_{out}}. \tag{2.36}$$

So assuming one to six CET coils with the individual component values of (2.17) as load and a rms output current of 1.32 A, the variation in output voltage amplitude and output power from the single coil unloaded to the six coil all maximum loaded situation becomes

$$\begin{aligned} B &\approx [0.61, 74.05]\ V, \\ P_{out} &\approx [0.73, 88.00]\ W. \end{aligned} \tag{2.37}$$

2.4 Power supply design

2.4.1 General

A nice way to produce the required square-wave output voltage of the power supply is by using a switch-mode inverter. The output voltage amplitude of this inverter is a constant value proportional to the dc input voltage of this inverter. Because the output voltage must be controllable, we are going to use the output of a step-down (or buck) converter as input of the inverter. Hereby, the output voltage of the inverter can be regulated from 0 to its maximum value by adjusting the switch duty ratio of the buck converter. To maintain the required constant rms sinusoidal output current, the switch duty ratio is controlled by a feedback control system. See figure 2.6 for the block diagram.

The AC-DC converter consists of an uncontrolled diode rectifier followed by a filter capacitor. Optionally, there is a battery connected to the input of the filter capacitor in case the line voltage power supply fails. For abstraction, we assume that the output of the AC-DC converter is available so that we initially can use a constant DC power source satisfying our needs.

In the next sections, each part of the block diagram will be described.

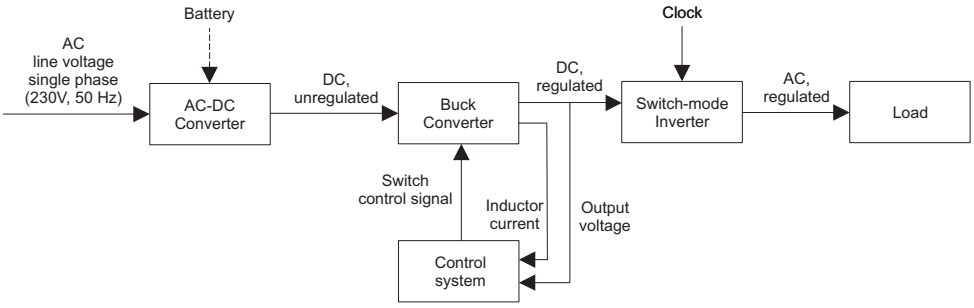


Figure 2.6: Block diagram of the CET power supply

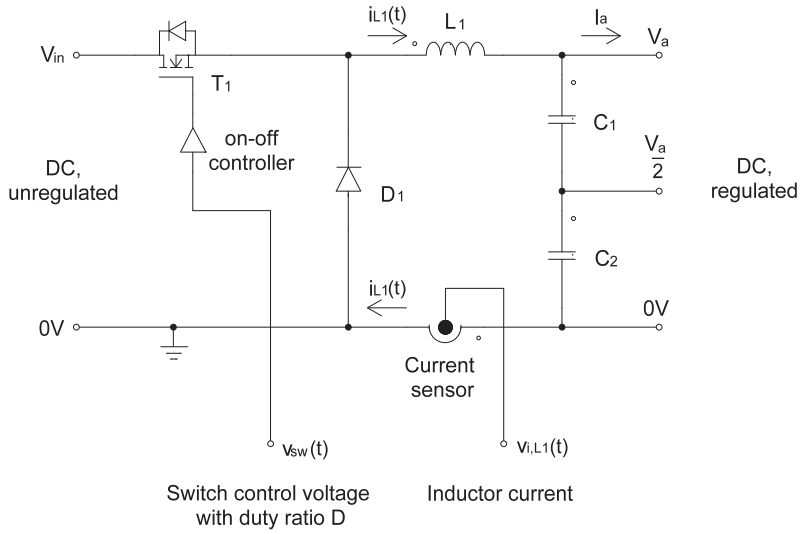


Figure 2.7: Circuit of the step-down converter

2.4.2 Buck converter

The buck converter produces a variable lower average dc output value V_a than the dc input voltage V_{in}, see figure 2.7.

MOSFET T_1 is used as a switch and his driving circuitry is abstracted by means of an on-off controller. Because we only need a switching component here, every suitable controllable switch can be used. Diode D_1 is needed to provide a path for the stored inductive energy in L_1 when switch T_1 is turned off. The square-wave voltage across diode D_1 consists of a dc component, and the harmonics at switching frequency $f_{s,buck}$ and its multiples. Because only the dc component is wanted, a low-pass filter is formed through inductor L_1 and the series equivalent capacitor of C_1 and C_2 to diminish this harmonics. There are two capacitors used instead of one, to supply for half the output voltage which will be needed lateron.

The average output voltage equals

$$V_a = DV_{in}, \tag{2.38}$$

with $D, \{D \in \mathbb{R} | 0 \leq D \leq 1\}$, equal to the switch duty ratio

$$D = \frac{t_{on}}{T_{s,buck}} = t_{on} f_{s,buck}. \tag{2.39}$$

The equivalent output capacitor, formed by the series connection of the 2 capacitors C_1 and C_2, equals

$$C_{buck,eq} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2}} = \frac{C_1 \cdot C_2}{C_1 + C_2}. \tag{2.40}$$

By recognizing that $V_{c_1} + V_{c_2} = V_a$ and $V_{c_2} = \frac{V_a}{2}$, we require that

$$C_1 = C_2, \tag{2.41}$$

so this implies that (2.40) now is equal to

$$C_{buck,eq} = \frac{C_1}{2} = \frac{C_2}{2}. \tag{2.42}$$

For the following, we assume that the converter operates in continuous conduction mode, i.e. the instantaneous current through L_1 will flow continuously, without being zero for a time period.

From [8], the percentage peak-to-peak output voltage ripple equals

$$r = \frac{\Delta V_a}{V_a} = \frac{1 - D}{8 f_{s,buck}^2 L_1 C_{buck,eq}}, \tag{2.43}$$

assuming that all of the ac ripple component in i_{L_1} flows through the capacitors and that $I_{a,avg} = I_{L_1,avg}$. This is a valid assumption because by definition, the average current through the capacitors over one time period equals zero.

Now, when we require a maximum output voltage ripple r_{max} for all possible values of D, we can calculate the minimum LC product to be

$$L_1 C_{buck,eq} \quad > \quad \frac{1}{8 r_{max} f_{s,buck}^2}. \tag{2.44}$$

When we assume the system is lossless and in steady state, we can state that the output power of the converter equals the load power. Also when we assume (as we will see later) that $V_a = 2B$ and that we have a n-coil load, the average current through L_1 can be calculated with help of (2.34), (2.35) and (2.36) as follows:

$$V_a I_{a,avg} = P_{out} \;\Leftrightarrow\; I_{L_1,avg} = I_{a,avg} \approx \frac{\sqrt{2}}{\pi} I_{out}. \tag{2.45}$$

Remark that this current is a constant because the output current I_{out} is constant.

We know, also from [8], that the inductor current variation equals

$$\Delta I_{L_1} = \frac{V_a (1 - D)}{f_{s,buck} L_1}. \tag{2.46}$$

So, when we want to remain in continuous conduction mode, for all possible values of D and by taking the maximum nR product, we can derive the following constraint for L_1:

$$I_{a,avg} - \frac{\Delta I_{L_1}}{2} > 0 \;\Leftrightarrow\; L_1 > \frac{\pi V_a}{\sqrt{8} I_{out} f_{s,buck}} \approx \frac{\pi^2 (nR)_{max}}{4 f_{s,buck}}. \tag{2.47}$$

Finally we can state that it is desirable to have an input voltage equal to the rectified line voltage, i.e. $V_{in} = 230\sqrt{2}\ V$. To check if this is possible, we calculate the interval in which D varies from the minimum possible loaded to the maximum possible loaded situation. Then, D must lay in the interval [0,1]. First, we will rewrite D with help of (2.38) and (2.34), assuming that the n load coils are equally loaded, as

$$\begin{aligned} D &= \frac{V_a}{V_{in}} \\ &\approx \frac{n\pi R I_{out}}{\sqrt{2}V_{in}}. \end{aligned} \tag{2.48}$$

Now, when we assume a rms output current of 1.32 A, a minimum load of one CET coil, unloaded, and a maximum load of six CET coils, maximum loaded, and with help of (2.17), D can be calculated to lay in the interval

$$\begin{aligned} D &\approx \frac{\pi I_{out}}{\sqrt{2}V_{in}} \left[(nR)_{min}, (nR)_{max}\right] \\ &\approx \frac{1.32\pi}{460}[0.4177, 50.5062] \\ &\approx [0.0038, 0.4553], \end{aligned} \tag{2.49}$$

so this satisfies the condition.

We now have all the equations we need to derive values for L_1, C_1 and C_2. With $n_{max} = 6$, $R_{max} = 8.4177\ \Omega$ and a switching frequency $f_{s,buck}$ of 50 kHz, (2.47) becomes

$$L_1 > 2.5\ mH. \tag{2.50}$$

With taking enough margin and a value of the E12 series, a legitimate inductor value would be to take

$$L_1 = 3.3\ mH. \tag{2.51}$$

When we want to have a maximum output voltage ripple of 0.1% with this inductor value, from (2.44), the equivalent output capacitor $C_{buck,eq}$ must be greater than

$$C_{buck,eq} > 15.2\ \mu F. \tag{2.52}$$

So, with (2.42), C_1 and C_2 must be greater than

$$C_1 = C_2 > 30.4\ \mu F. \tag{2.53}$$

With taking enough margin, valid capacitor values of the E12 series would yield

$$C_1 = C_2 = 47\ \mu F. \tag{2.54}$$

2.4.3 Switch-mode inverter

Because we control the dc input voltage of this inverter in order to control the magnitude of the square-wave output ac voltage, our inverter will be a square-wave voltage source inverter with a constant frequency. See figure 2.8 for the circuit.

MOSFETs T_2 and T_3 are acting as switches with abstracted driving circuitry by means of on-off controllers. Again, every suitable controllable switch can be used here. The gate signals are obtained by an external 2.78 MHz clock signal with duty ratio $\frac{1}{2}$. By means of the logic inverter, both switches can never be on simultaneously.

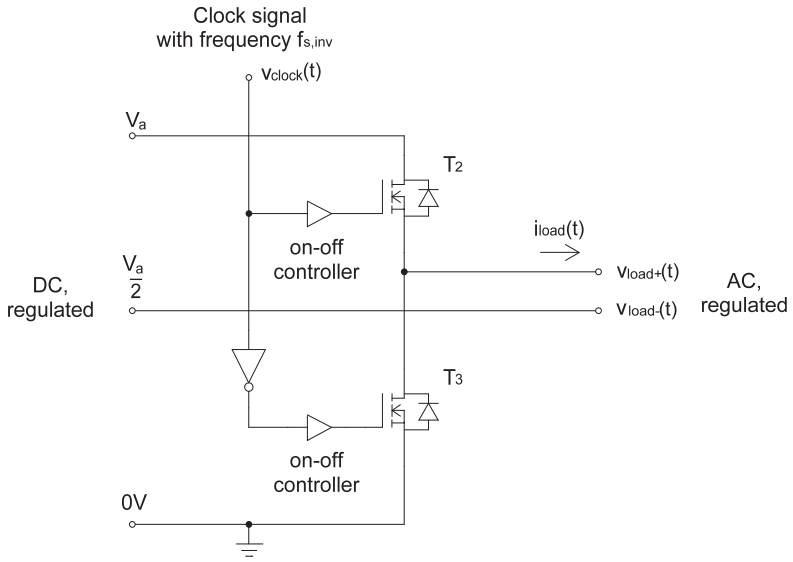


Figure 2.8: Inverter circuit

In order to eliminate the switching losses in the gate drive circuits of MOSFETs T_2 and T_3, which is caused by the high switching frequency and the internal gate capacitances of the MOSFETs, the use of resonant gate driving is recommended. A detailed analysis of the resonant gate drive in comparison to the conventional gate drive can be found in [7]. Other recommended readings about this topic are [10] and [4].

With $T_{s,inv} = \frac{1}{f_{s,inv}}$, the instantaneous output load voltage can be calculated to be

$$\begin{aligned} v_{load}(t) &= v_{load_+}(t) - v_{load_-}(t) \\ &= \begin{cases} \frac{V_a}{2}, & 0 < (t \bmod T_{s,inv}) < \frac{T_{s,inv}}{2} \\ -\frac{V_a}{2}, & \frac{T_{s,inv}}{2} < (t \bmod T_{s,inv}) < T_{s,inv}. \end{cases} \end{aligned} \tag{2.55}$$

When we define $B = \frac{V_a}{2}$, $T_{res} = T_{s,inv}$ and $v_{out} = v_{load}$, equation (2.18) is obtained.

2.4.4 Load

The load will consist of a series connection of n CET coils, as in figure 2.4. The individual coil values equal (2.17). When we define $v_{coils} = v_{load}$ and $i_{coils} = i_{load}$, the analysis of section 2.2.3 holds.

2.4.5 Control system

We are going to use a current-mode control system to maintain the desired constant load current. By doing this, we are directly controlling the inductor current of the buck converter.

There are several types of current-mode controls. Because we are using a constant switching frequency $f_{s,buck}$ of the buck converter, the constant-frequency control with turn-on at clock time will be the type we are going to use, see figure 2.9.

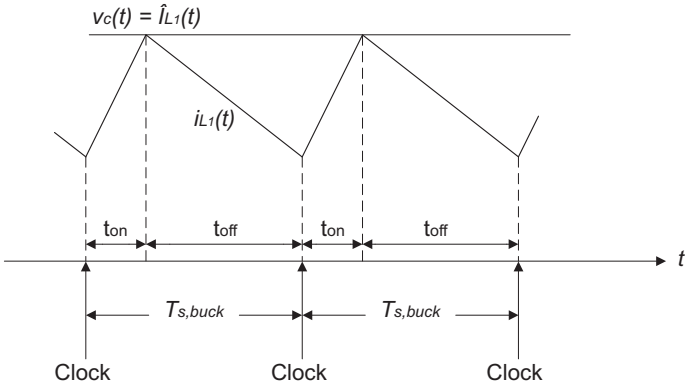


Figure 2.9: Constant frequency with turn-on at clock time current-mode control

From the instantaneous output voltage $V_a(t)$ of the buck converter, which is fed back, a control voltage $v_c(t)$ is derived. This control voltage depicts the desired $\hat{I}_{L_1}(t)$ of the buck converter and equals

$$\begin{aligned} v_c(t) \;=\; \hat{I}_{L_1}(t) \;=\; f(V_a(t)) \;&=\; I_{L_1,avg} + \frac{1}{2}\Delta I_{L_1}(t) \\ &=\; \frac{\sqrt{2}}{\pi} I_{out} + \frac{V_a(t)\left(1 - \frac{V_a(t)}{V_{in}}\right)}{2 f_{s,buck} L_1}, \end{aligned} \tag{2.56}$$

with I_{out} taken as a constant, i.e. the desired steady state value (so not the fed back output current).

Next, this control voltage is compared with the actual inductor current $i_{L_1}(t)$ of the buck converter.

At the beginning of each frequency switching time period, i.e. at the rising edge of the clock signal with time period $T_{s,buck}$, the output switch control signal becomes high if $i_{L_1}(t) < v_c(t)$ and hence, the switch is turned on. When the actual inductor current reaches the value of the control voltage, the switch control signal becomes zero, so the switch is turned off. The switch remains off until the next switching cycle begins, when there is a new rising edge of the clock signal.

When we now define $E_{control}(t)$, for which holds that

$$E_{control}(t) = \begin{cases} 0, & i_{L_1}(t) < v_c(t) \\ 1, & i_{L_1}(t) \geq v_c(t) \end{cases}, \tag{2.57}$$

we can make the following truth table for a logic element with binary inputs $Clock$ and $E = E_{control}(t)$ and with switch duty ratio output Q (0 and 1 means the switch will be off and on, respectively), assuming $E = 0$ during the rising edge of the clock pulse:

Table 2.1: Truth table logic element

Clock	E	Q
0	0	unchanged
0	↑	0
↑	0	1

As can be seen from the table, we can use an edge-triggered Set-Reset Flip-Flop with set input $S = Clock$ and reset input $R = E$ as logic element having the desired behavior. Remark that the forbidden situation of $R = S =\uparrow$ can never occur.

From (2.49) and (2.39), the minimum time the switch of the buck converter will be on equals

$$t_{on,min} \approx \frac{\pi I_{out}}{\sqrt{2}\, V_{in} f_{s,buck}} (nR)_{min}\,, \tag{2.58}$$

so $E_{control}(t)$ will be zero for at least the time $t_{on,min}$ takes after a clock pulse was given. After this time, $E_{control}(t)$ can become high. So for the Flip-Flop to operate properly, the clock input must be high for at most the time $t_{on,min}$ takes, to ensure the clock input is zero when $E_{control}(t)$ becomes high. Therefore, we must define $t_1 < t_{on,min}$, where t_1 denotes the time the clock signal is high; see figure 2.10.

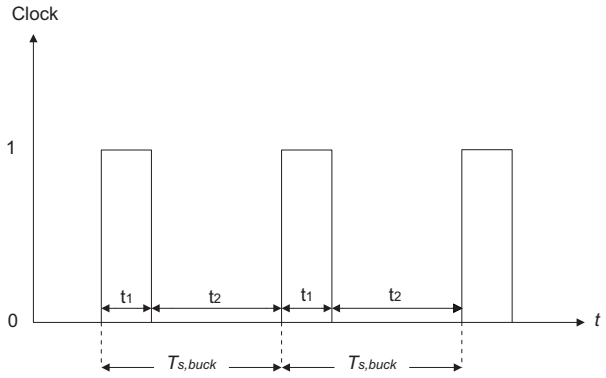


Figure 2.10: Internal clock signal of the control system

See figure 2.11 for the total circuit of the control system.

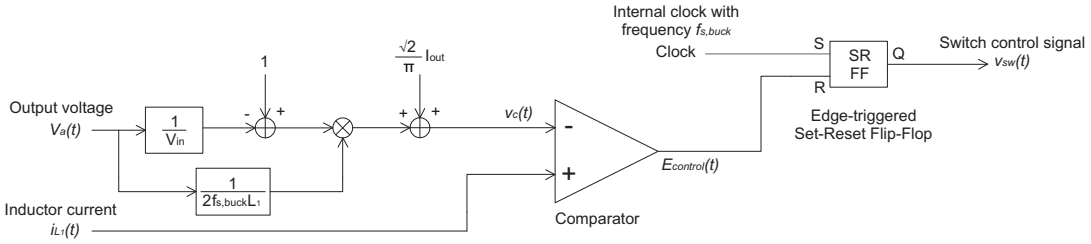


Figure 2.11: Circuit of the control system

2.4.6 Complete power supply analysis

In this section, we will analyze the effect of a stepwise load change and calculate the input power (and thereby, the performance) of the complete power supply.

Stepwise load change

Now we will analyze the impact of the worst-case scenario of a load change which is a stepwise change in the total equivalent series output load resistance value. Hereby, we assume that the system is in steady state for the current load value.

First, we observe that the voltage V_a (and hence B, which equals $\frac{V_a}{2}$) can not change stepwise, as by definition is the case about the voltage across a capacitor. The same can be said about the current through the inductor L_1. So after a stepwise load change, the control voltage v_c, which depends on constant values and V_a, will initially be the same as the previous steady state value.

Also, the rise time of the inductor current $\frac{di_{L_1}}{dt}$, which equals $\frac{V_{in}-V_a}{L_1}$, will initially not change after a load change. Therefore, the switch duty ratio output of the control system initially will not change. Now, the two scenario's of a load change can be worked out as follows.

In the first scenario, the load will stepwise increase. By definition of Ohm's law, the output load current is inversely proportional to the equivalent series output load resistance, so the output load current will stepwise decrease. Because $Q_c = I_c \cdot t$, the capacitors C_1 and C_2 now will be less discharged per cycle in comparison with the previous steady state situation. Looking at figure 2.9, we can now state that after the switch is turned off, so at the time instant at which the inductor current equals the control voltage, the charge of the capacitors must be increased. Therefore, by $Q_c = C \cdot V_c$, the voltage V_a must also be increased. With an increasing V_a, v_c will increase if

$$\begin{aligned}
(V_a + \Delta V_a)\left(1 - \frac{V_a + \Delta V_a}{V_{in}}\right) &> V_a\left(1 - \frac{V_a}{V_{in}}\right) \qquad (2.59)\\
\Delta V_a - \frac{(V_a + \Delta V_a)(V_a + \Delta V_a)}{V_{in}} &> -\frac{V_a^2}{V_{in}}\\
\Delta V_a - \frac{2V_a\Delta V_a + (\Delta V_a)^2}{V_{in}} &> 0\\
\frac{2V_a + \Delta V_a}{V_{in}} &< 1\\
D &< \frac{1}{2} - \frac{\Delta V_a}{2V_{in}},
\end{aligned}$$

and because $\Delta V_a << V_{in}$, the constraint becomes

$$D < \frac{1}{2}. \qquad (2.60)$$

Because of (2.49), this is always the case.

Now, by the increase of V_a, the rise time of the inductor current will decrease. Both the increasing v_c and decreasing $\frac{di_{L_1}}{dt}$ are contributing to an increasing t_{on}, and so the buck converter duty cycle and hence the output load voltage will increase. Hereby, the output current will also increase. This will continue until the duty ratio has reached its final steady state value and thereby, the output load voltage is adjusted to acquire the required output current I_{out}.

In the second scenario, the load will stepwise decrease. The inverse of the load increase situation will now happen. By Ohm's law, the output load current will stepwise increase. The capacitors C_1 and C_2 will now be more discharged per cycle. Therefore, the charge of the capacitors must be decreased at the time instant at which the instantaneous inductor current equals the control voltage. Thus, the voltage V_a must also be decreased and so also the output load current. Control voltage v_c will also decrease if

$$\begin{aligned}
(V_a - \Delta V_a)\left(1 - \frac{V_a - \Delta V_a}{V_{in}}\right) &< V_a\left(1 - \frac{V_a}{V_{in}}\right) \qquad (2.61)\\
-\Delta V_a - \frac{-2V_a\Delta V_a + (\Delta V_a)^2}{V_{in}} &< 0\\
2D - \frac{\Delta V_a}{V_{in}} &< 1\\
D &< \frac{1}{2} + \frac{\Delta V_a}{2V_{in}},
\end{aligned}$$

and with $\Delta V_a << V_{in}$, the constraint becomes again (2.60) which is always satisfied by (2.49).

By the decrease of V_a, the rise time of the inductor current will increase. Both the decreasing v_c and increasing $\frac{di_{L_1}}{dt}$ are contributing to an decreasing t_{on}, so the duty cycle of the buck converter and hence the output load voltage and current will decrease. This will continue until the new final steady state situation is reached.

Input power and efficiency

The total power drawn from the input DC voltage equals

$$P_{in} = V_{in} I_{in,avg}. \tag{2.62}$$

Because the input current is only flowing through T_1 when this switch is on, and when this is the case, this input current equals the inductor current, the average input current can be written as

$$\begin{aligned} I_{in,avg} &= \frac{t_{on}}{T_{s,buck}} I_{L_1} \\ &= D I_{L_1} \\ &\approx \frac{V_a}{V_{in}} \cdot \frac{\sqrt{2}}{\pi} I_{out} \\ &= \frac{2B\sqrt{2} I_{out}}{\pi V_{in}} \\ &\approx \frac{I_{out}^2 \left(R_{C_1} + R_{C_2} + \ldots + R_{C_n}\right)}{V_{in}}. \end{aligned} \tag{2.63}$$

So, (2.62) becomes

$$P_{in} \approx I_{out}^2 \left(R_{C_1} + R_{C_2} + \ldots + R_{C_n}\right), \tag{2.64}$$

and this is equal to (2.36), i.e. the output power. This implies an efficiency of 100%, but, of course, this is a theoretical value with the use of ideal components under ideal circumstances. Nevertheless, a high efficiency of the power supply should be possible.

Because the instantaneous input current waveform jumps from a peak value to zero every time the switch is turned off, it can be desirable to place an appropriate filter at the input to eliminate the effects of the current harmonics.

Chapter 3

Simulation

In this chapter, the simulation results are presented of the complete power supply. The modelling and simulation are done in PSIM 7.0. There is chosen to simulate the complete power supply instead of a simulation of all the separate (trivial) components. In this way, the collaboration of all the subelements and the global performance can be analyzed.

We assume a dc rectified line input voltage of $230\sqrt{2}$ V, the individual derived component values for L_1, C_1 and C_2, a desired rms output current of 1.32 A and a switching frequency of the buck converter of 50 kHz.

From section 2.4 and its subsections, the total power supply model is made; see figure 3.1.

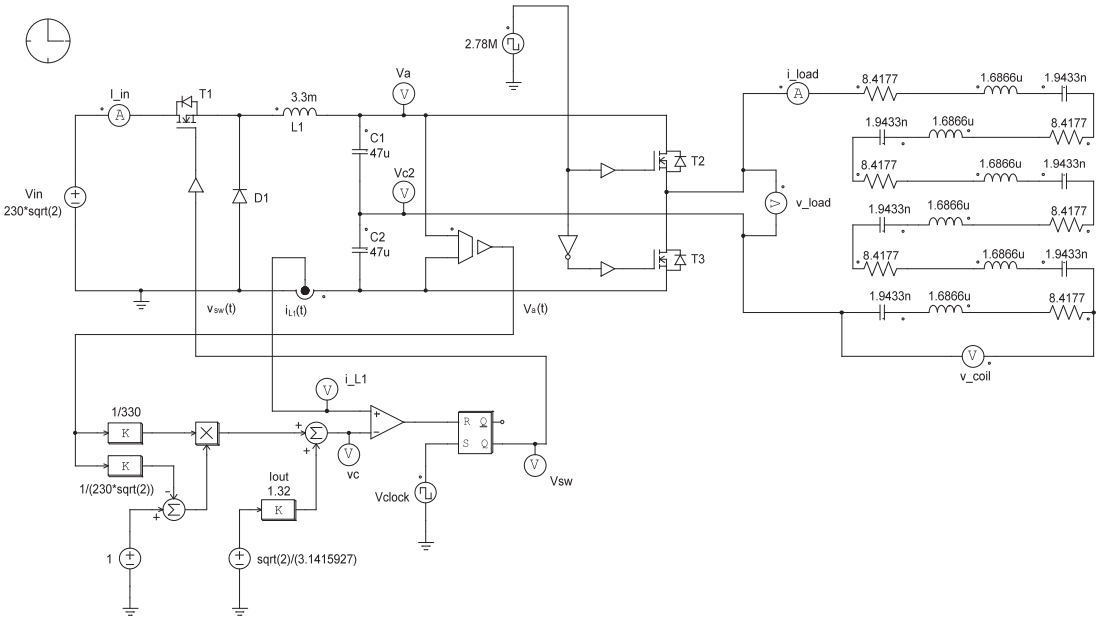


Figure 3.1: PSIM power supply model

The output load of the power supply in the model consists of six maximum loaded CET coils. Of course, the number of coils and the amount of loading of the individual coils could differ from this model. Therefore, the two load extremes which can occur will be simulated, i.e. one coil, minimum loaded and six coils, maximum loaded with all the coils having the individual component values of (2.17). Also, the stepwise transition from one extreme to the other and vice versa will be simulated to see the impact of a worst case stepwise load change.

3.1 Minimum load

See figure 3.2 for the simulation results of the minimum loaded power supply from starting up till steady state.

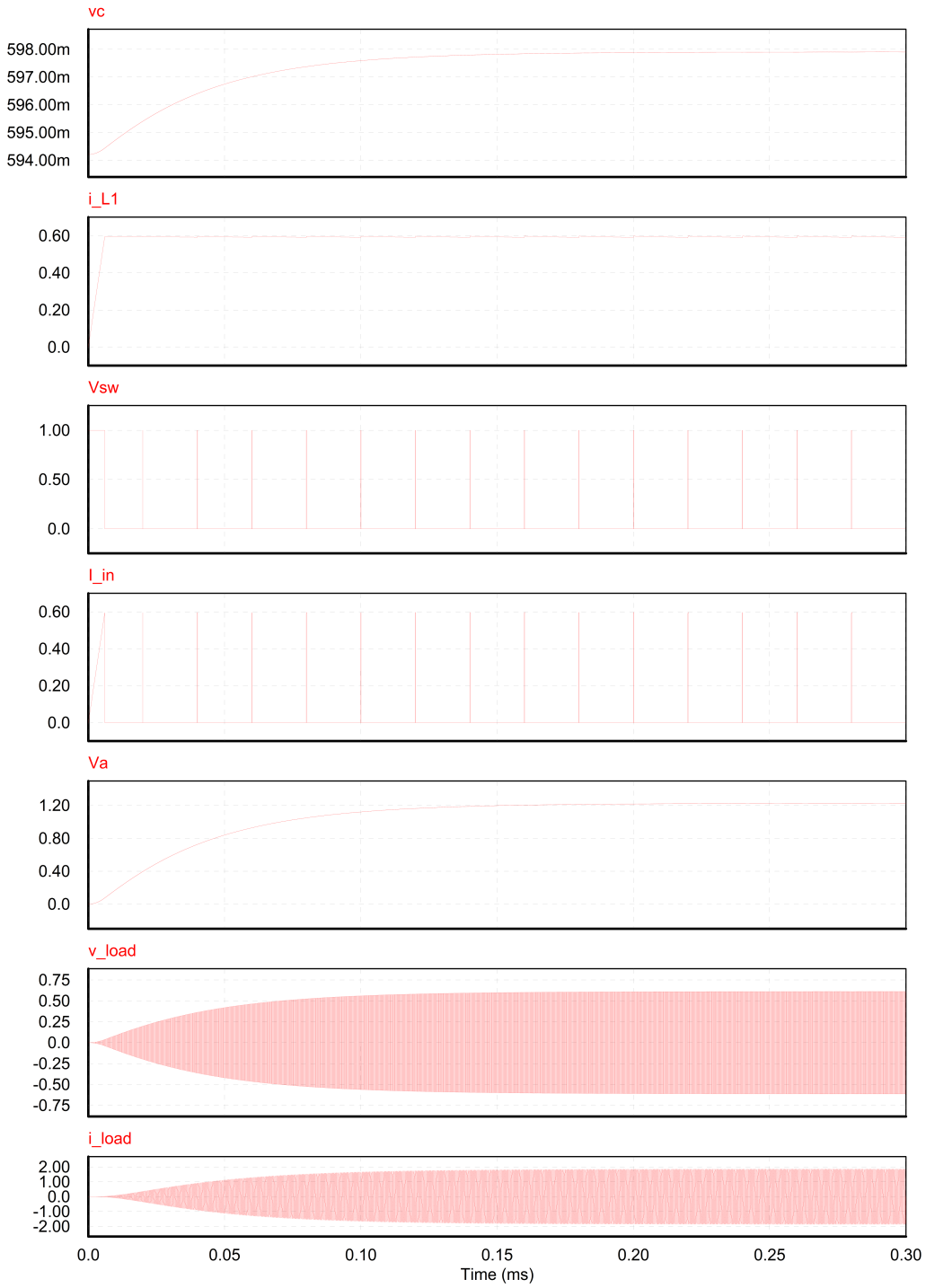


Figure 3.2: Simulation results minimum loaded power supply

We notice that during startup, the input current is continuously increasing to its steady state pulse value, without overshoot. The startup time of the power supply equals approximately 250 μs. The steady state waveforms are presented in figure 3.3.

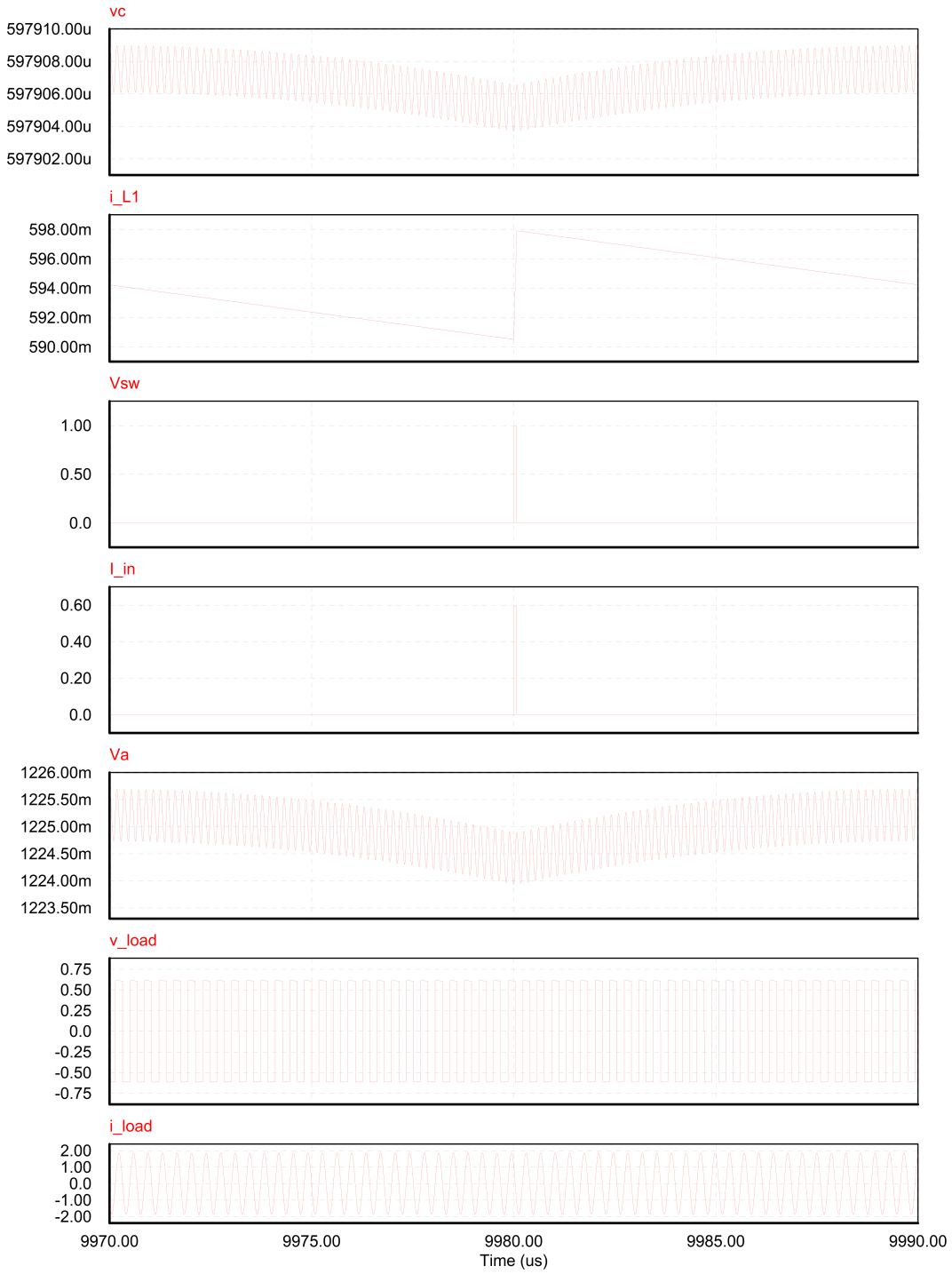


Figure 3.3: Steady state simulation results minimum loaded power supply

The steady state output voltage and current waveforms can be found in figure 3.4.

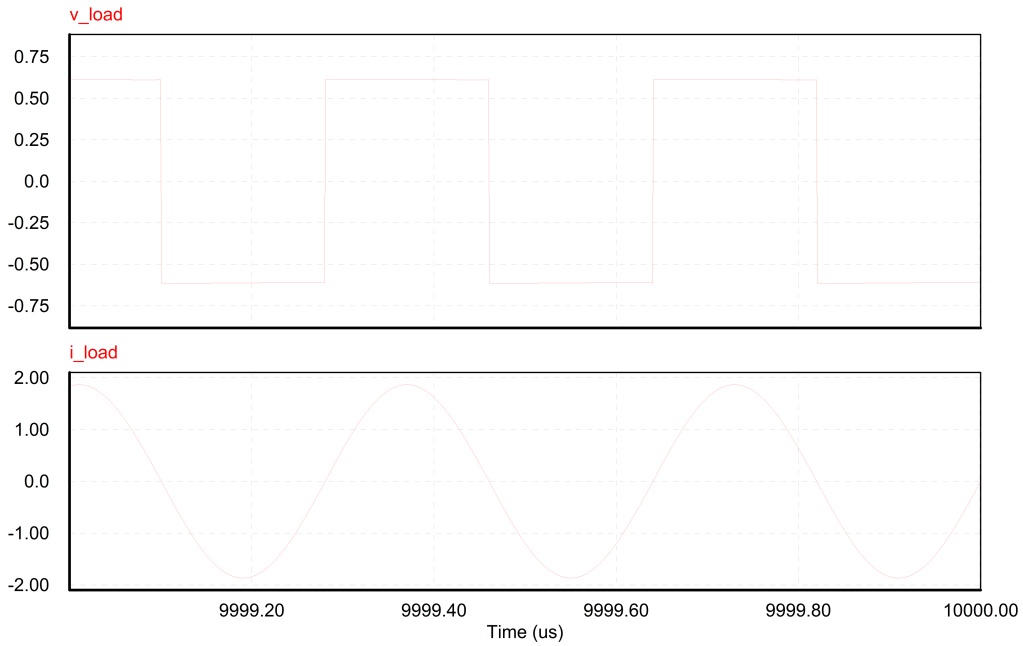


Figure 3.4: Steady state output current and voltage waveforms minimum loaded power supply

The output voltage is clearly square-wave and the output current has a nice, smooth sinusoidal waveform.

From the steady state simulation results, the following values are extracted:

- $I_{L_1,avg} \approx 594.22$ mA and $\Delta I_{L_1} \approx 7.40$ mA (remark that (2.47) is satisfied)
- $I_{in,avg} \approx 2.29$ mA and so $P_{in} \approx 744.87$ mW
- $V_a \approx 1.23$ V, $\Delta V_a \approx 0.80$ mV and so $r \approx 0.065$ % (remark that $r < 0.1$ %)
- $V_{load} \approx 613.85$ mV and so $V_{load_1} \approx 552.66$ mV
- $I_{load} \approx 1.32$ A and so $P_{load} \approx 729.51$ mW

3.2 Maximum load

See figure 3.5 for the simulation results of the maximum loaded power supply from starting up till steady state.

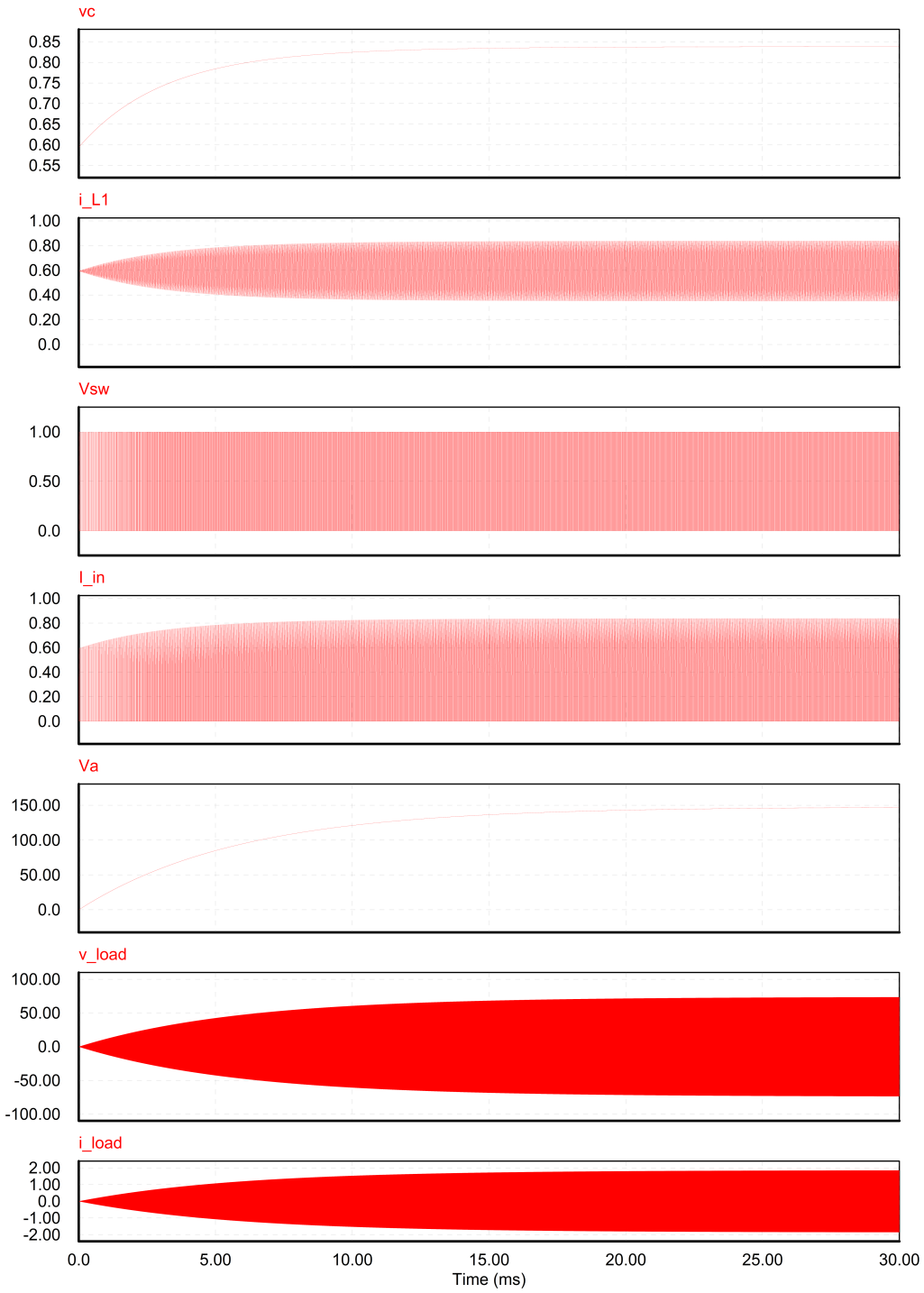


Figure 3.5: Simulation results maximum loaded power supply

The startup time of the power supply equals approximately 30 ms. For clearance, in figure 3.6, the starting up of the power supply is depicted.

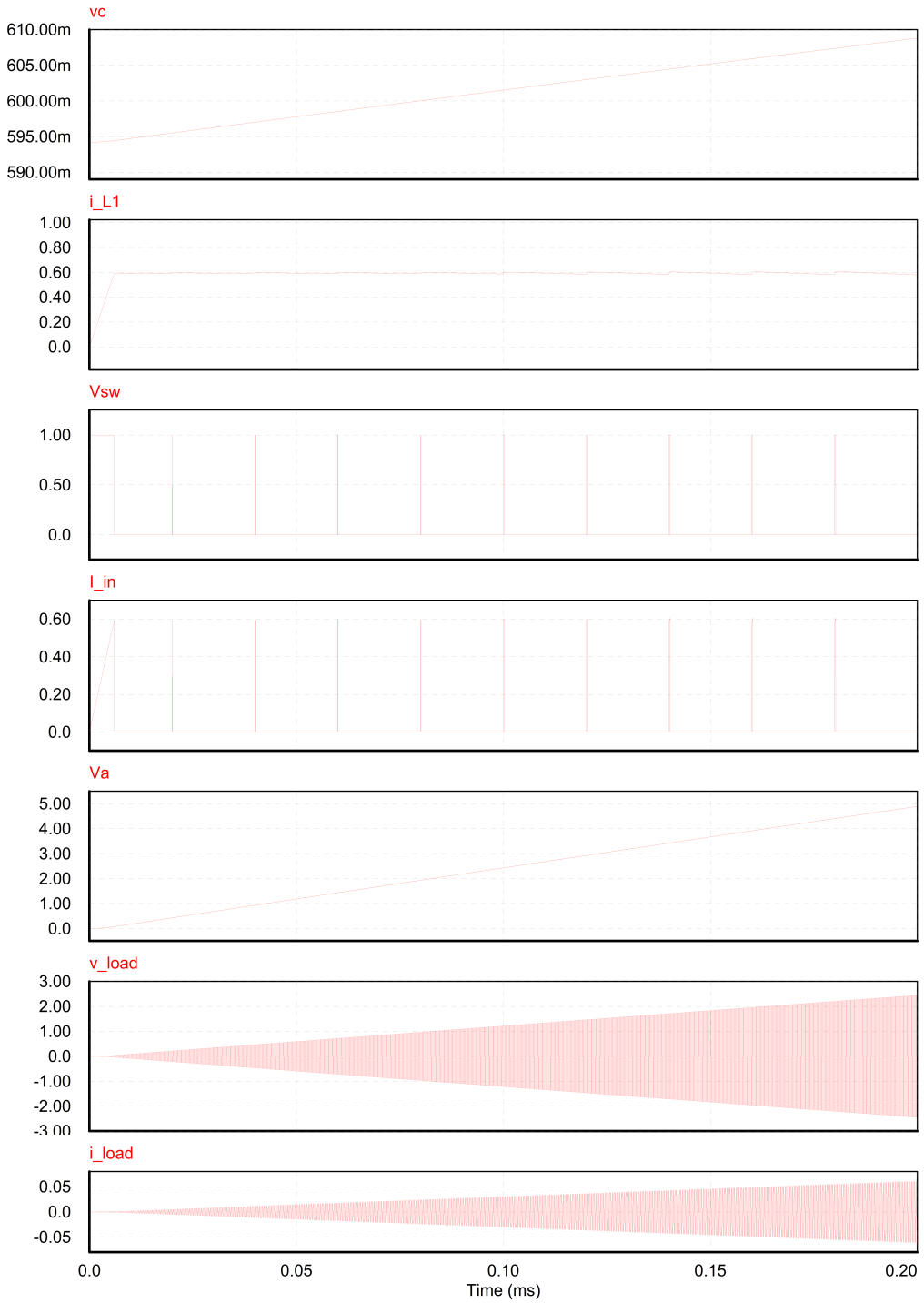


Figure 3.6: Simulation results maximum loaded power supply during startup

Again, the input current is continuously increasing to its steady state pulse value, without overshoot. The steady state waveforms are presented in figure 3.7.

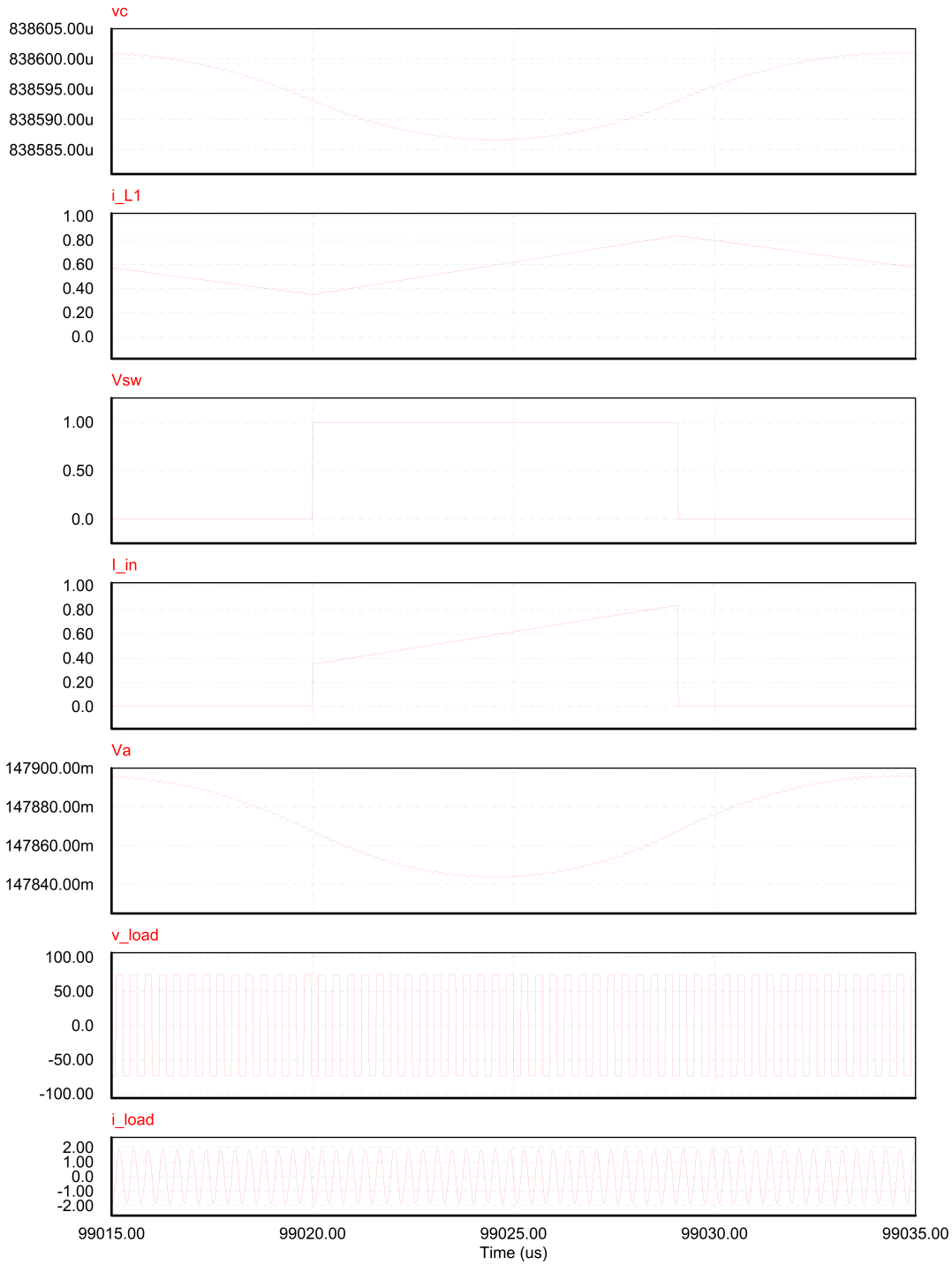


Figure 3.7: Steady state simulation results maximum loaded power supply

The steady state output voltage and current waveforms are depicted in figure 3.8, and the steady state output voltage and single coil voltage can be found in figure 3.9.

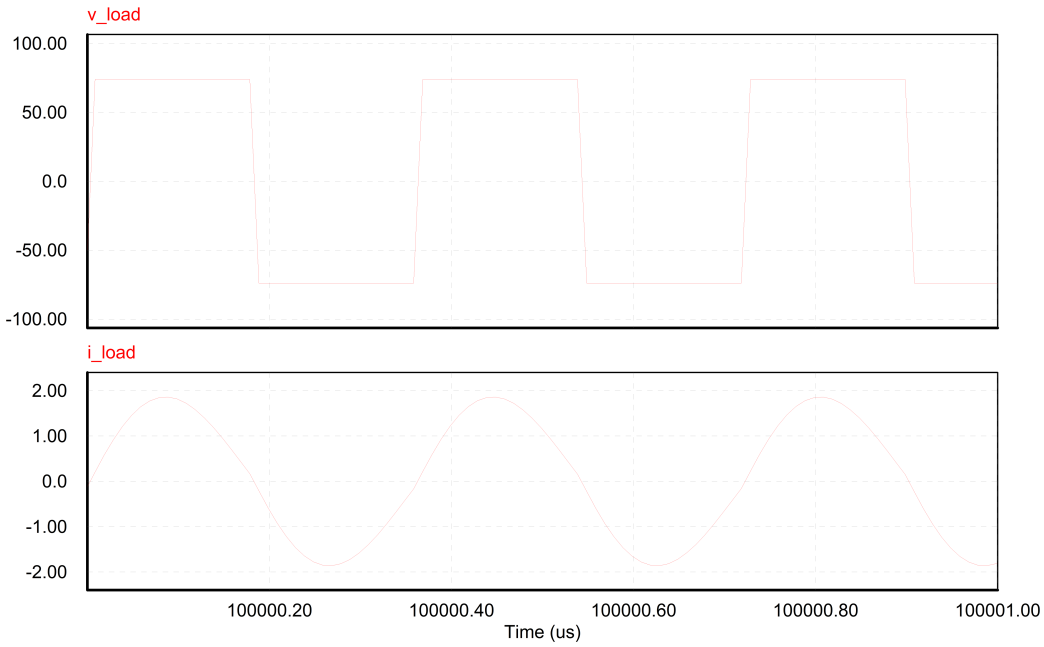


Figure 3.8: Steady state output voltage and current waveforms maximum loaded power supply

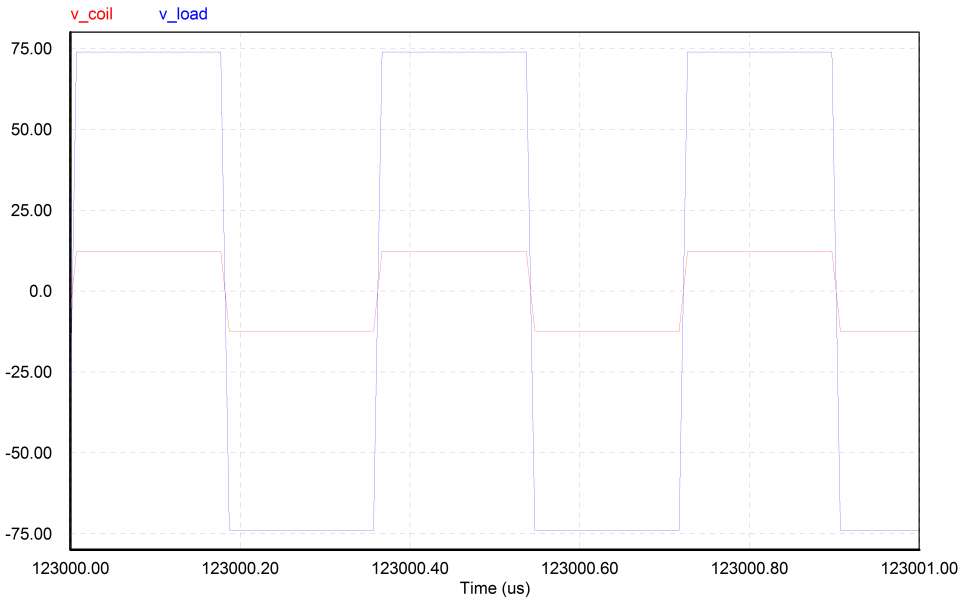


Figure 3.9: Steady state output and single coil voltage waveforms maximum loaded power supply

We see that the voltage across a single coil indeed approximates one sixth of the output voltage, because of the equal loading of the individual coils.

Note that the sinusoidal output current is slightly distorted, due to the existence of odd upper harmonic components which are now, compared to the minimal load situation, less suppressed. Also be noted that in this simulation the logging of the simulation results was reduced by a factor 10 in comparison with the minimal loaded situation. As a result of this, the rise and fall times in the representation of the output voltage in figures 3.8 and 3.9 are slightly increased.

From the steady state simulation results, the following values are extracted:

- $I_{L_1,avg} \approx 594.17$ mA and $\Delta I_{L_1} \approx 488.55$ mA (remark that (2.47) is satisfied)
- $I_{in,avg} \approx 269.90$ mA and so $P_{in} \approx 87.79$ W
- $V_a \approx 147.87$ V, $\Delta V_a \approx 53$ mV and so $r \approx 0.036$ % (remark that $r < 0.1$ %)
- $V_{coil} \approx 12.32$ V, $V_{load} \approx 73.93$ V and so $V_{load_1} \approx 66.56$ V
- $I_{load} \approx 1.32$ A and so $P_{load} \approx 87.64$ W

3.3 Stepwise minimum to maximum load change

In this section, a stepwise load change from the minimum (i.e. a single coil, unloaded) to the maximum (i.e. six coils, maximum loaded) possible value will be simulated. The change in the load occurs at t=1 ms, when the power supply is in steady state due to the unloaded single coil as load. See figure 3.10 for the total simulation results.

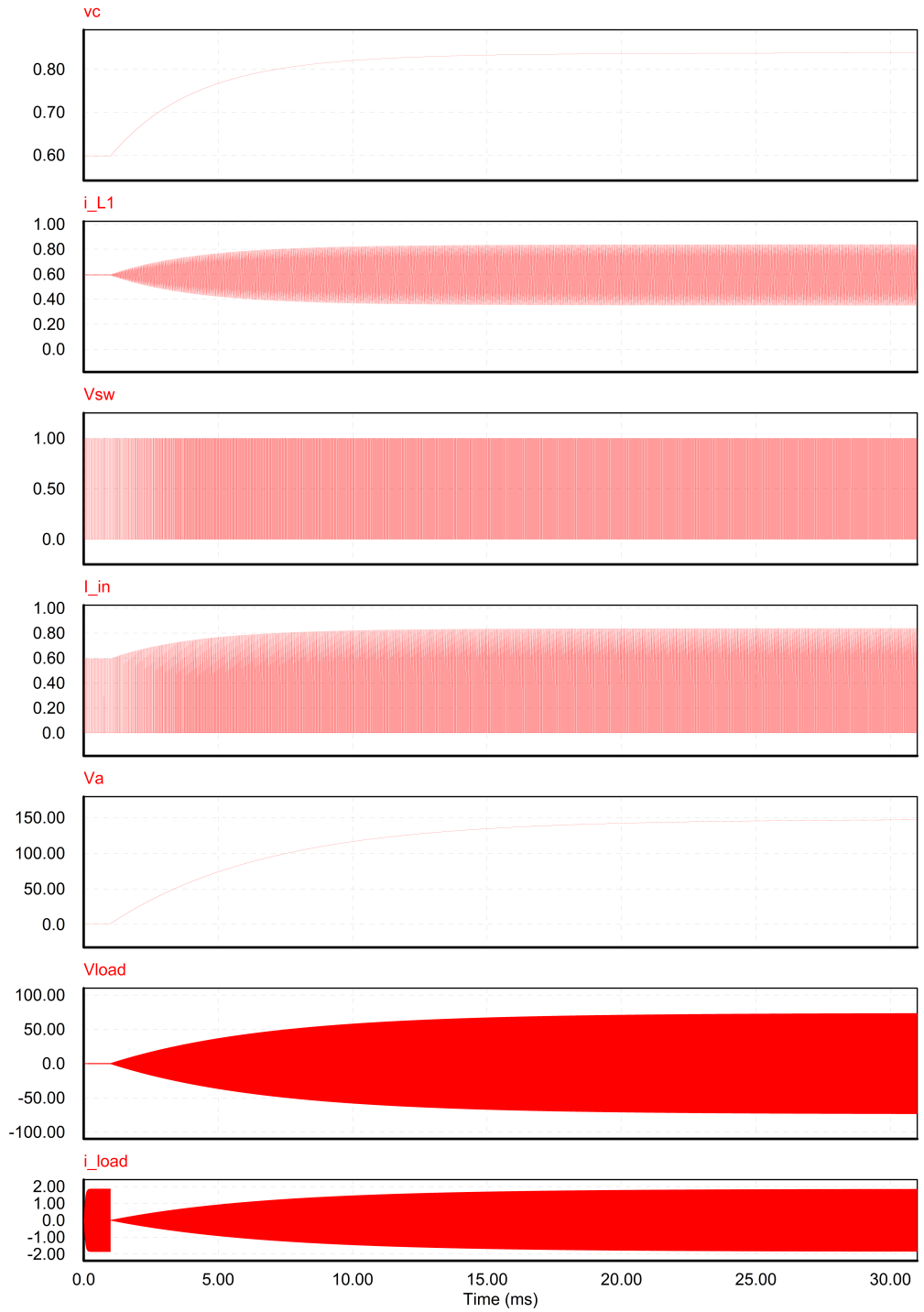


Figure 3.10: Simulation results stepwise minimum to maximum load change at t=1 ms

We see that, during the transition, the output current is falling to a (nearly) zero value and afterwards is climbing to its steady state value while the output voltage just slowly rises to its desired value, exactly as expected. Likewise, V_a and v_c are increasing. It takes about 30 ms for the system to reach its final steady state after the transition which is, of course, exactly the same as we saw earlier in the maximum loaded situation.

A close-up view of the impact of the stepwise load change is depicted in figure 3.11.

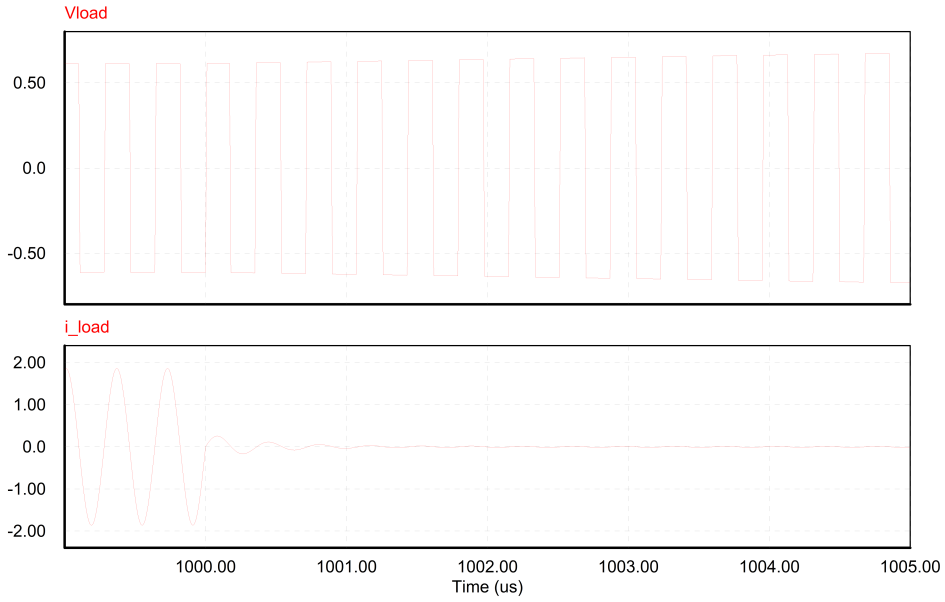


Figure 3.11: Impact of min-to-max loaded transition at t=1 ms

3.4 Stepwise maximum to minimum load change

Finally, we are going to simulate a stepwise load change from the maximum to the minimum possible value. That is, from a load consisting of six coils, maximum loaded to a single coil, unloaded. The stepwise change in the load occurs at t=50 ms, when the power supply has reached its maximum loaded steady state. See figure 3.12 for the total simulation results.

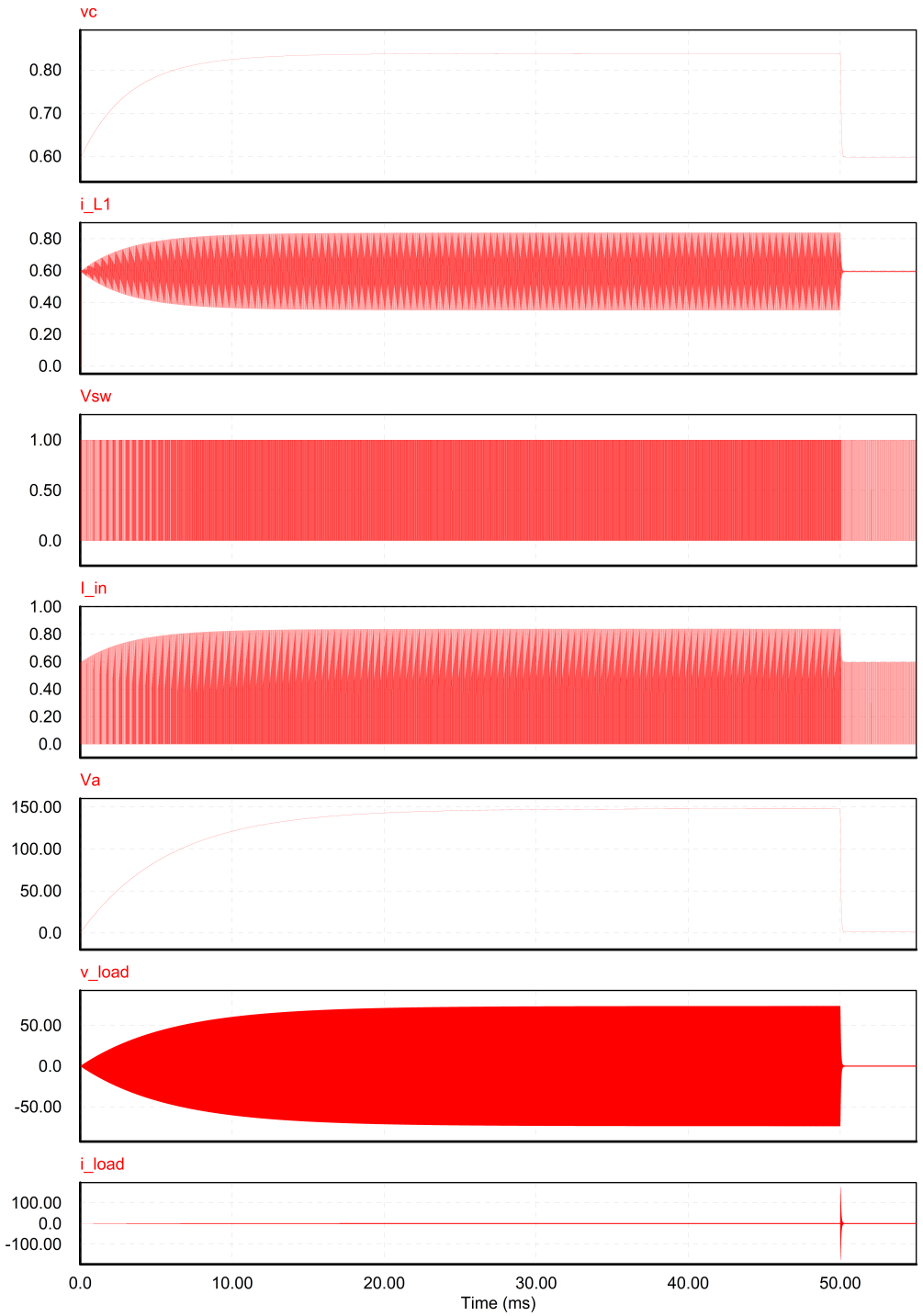


Figure 3.12: Simulation results stepwise maximum to minimum load change at t=50 ms

Here we see that, during the transition, the output current is inevitable rising very fast to a very high value for a short period of time. Fortunately, the current control system very rapidly reacts and as a result of that, the output current suddenly decreases very fast to its desired constant steady state value. V_a, v_c and the output voltage are also decreasing to the new final steady state value, as expected. The total time it takes for the system to reach its new steady state after the transition is about 300 μs.

See figure 3.13 for a close-up view of the impact of the stepwise load change.

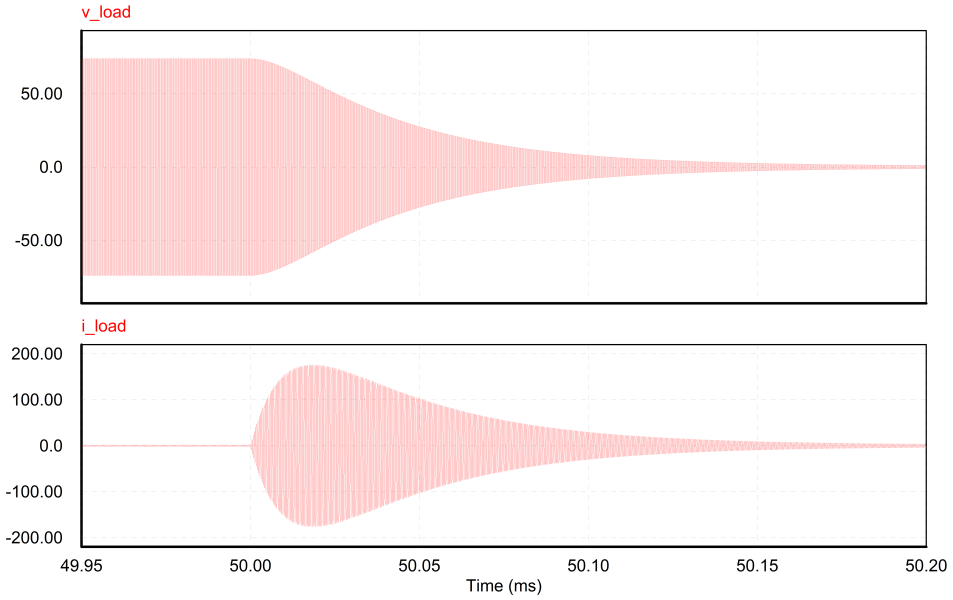


Figure 3.13: Impact of max-to-min loaded transition at t=50 ms

Chapter 4

Theory and simulation differences

Now we are going to compare the simulation results with the theoretical calculated values of the system variables; both outcomes should lay close to eachother. See table 4.1 for the comparison.

Table 4.1: Theory vs. simulation results

Variable	Min load (th.)	Min load (sim.)	Max load (th.)	Max load (sim.)
$I_{L_1,avg}$ [mA]	594.21	594.22	594.21	594.17
ΔI_{L_1} [mA]	7.40	7.40	488.90	488.55
$I_{in,avg}$ [mA]	2.24	2.29	270.55	269.90
P_{in} [W]	0.73	0.74	88.00	87.79
V_a [V]	1.22	1.23	148.10	147.87
ΔV_a [mV]	0.79	0.80	52.01	53.00
r [%]	0.064	0.065	0.035	0.036
V_{load} [V]	0.61	0.61	74.05	73.93
I_{load} [A]	1.32	1.32	1.32	1.32
P_{load} [W]	0.73	0.73	88.00	87.64
η [%]	100.00	97.94	100.00	99.83

As can be seen, the differences are minimal ($< 3\%$) and are most likely caused by reading errors and rounding errors. There is no major difference which needs to be further analyzed.

Chapter 5

Conclusion

The power supply for the CET project presented in this report consists of the following elements:

- AC-DC converter which consists of an uncontrolled diode rectifier followed by a filter capacitor to obtain an unregulated dc voltage of approximately 325 V ($=230\sqrt{2}$).
- Buck converter which is controlled by a (output current) control system, with the unregulated dc voltage as input, supplying the needed regulated dc voltage such that the desired output load current is respected and maintained. The switching frequency of this converter is chosen to be 50 kHz, a regular value. By making use of a capacitor voltage divider, half of the regulated dc voltage is also available, creating a virtual zero voltage point.
- Switch-mode inverter with the regulated dc voltages as input, controlled by an external clock with a frequency of 2.78 MHz, to obtain the square-wave ac output voltage with duty cycle 50% for powering the CET coils.
- Current control system with the measured output voltage and the buck converter inductor current as input, generating the switch duty ratio signal for the buck converter, such that the (adjustable) desired output load current is respected and maintained.

The output current is very easily adjustable by changing a constant value in the circuit of the current control system. And like summarized, the power supply switching rate, which is controlled by the switch-mode inverter, is driven by the external clock signal. The theoretical achievable efficiency approaches 100% and the theoretical and simulation results match with a relative error less than 3%, most likely caused due to rounding and reading errors.

The output load CET coils, resonant at 2.78 MHz, are all assumed to have the following component values:

- $L_C = 1.6866\ \mu H$
- $C_C = 1.9433\ nF$
- $R_C = [no\ load,\ max\ load] = [0.4177, 8.4177]\ \Omega$

Assuming zero initial conditions, the starting-up times of the power supply, i.e. the time it takes to become in steady state after the power supply is switched on with some loading, are as follows:

- Minimum loaded (one coil, unloaded): 250 μs without overshoot during transient
- Maximum loaded (six coils, maximum loaded): 30 ms without overshoot during transient

When the load is stepwise changing (worst possible case scenario), the systems reacts as follows:

- Stepwise change from minimum (one coil, unloaded) to maximum (six coils, maximum loaded) possible load: No transient overshoot, output voltage slowly rises to its steady state value and the output current stepwise decreases, followed by an increase to its steady state value. The total time it takes to become in steady state again after the stepwise load change is 30 ms.
- Stepwise change from maximum (six coils, maximum loaded) to minimum (one coil, unloaded) possible load: Only the output current has a big, but short, transient overshoot. The current control system rapidly regulates this output current back to its constant steady state value. The output voltage doesn't jump stepwise, but just slowly decreases to its steady state value. The total transient time to become in the new steady state after the stepwise load change is 300 μs.

Chapter 6

Future work and recommendations

For the people following up this work, here are a couple of notes:

1. Because the instantaneous input current waveform jumps from a peak value to zero every time the switch of the buck converter is turned off and the switching frequency equals 50 kHz, it can be desirable to place an input filter to eliminate this unwanted current harmonics.
2. It may be convenient to investigate the effect of a no-loaded power supply, i.e. a power supply without anything connected to the output, especially during startup.
3. It may be the case that the buck converter switch duty ratio has an upper limit of 0.5, because of (2.59) and (2.61). So the need arises to analyze the behavior of the power supply if this ratio exceeds 0.5.
4. From [9], in practice, it is recommended to place (high valued) resistors in parallel with the capacitors of the capacitor voltage divider at the output of the buck converter to balance the voltages.

Appendix A

Time table

Week 36

Arranged some books which could be helpful and read several chapters [8][9]. It was helpful to review some basic electric concepts and to work out formulas and examples from the book. Some electrical diagrams of switched power supplies were collected which could serve as practical examples. On the Internet I found some good free online datasheet catalog for electronic components and semiconductors [2]. I discovered that there exist semiconductors for e.g. power MOSFET driving, control circuitry and PWM control. Some example datasheets were collected. Of course, that specific semiconductor devices may not fulfil our requirements yet, but it's a good starting point if we need some lateron. From the magazine Elektor, some switched power supply articles are collected. In Matlab, I made some figures to experiment (e.g. the impedance of one coil as function of the frequency). I made a start with the report in MS Word, and wrote down some of the findings so far. I also tried to discover how good the higher harmonic current components are suppressed by the series resonance band-pass filter. The effect of multiple connected coils (with respect to the output voltage amplitude, the resonance frequency and the LC product) was analyzed. I installed myself at my working place at the university and got acquainted with my colleague students.

Week 37

I read the miniPE document [6]. Made a initial PSIM model and showed it to my supervisors which gave me feedback. I decided to learn the typesetting system LaTeX; handy for now and for the Master's thesis later. I printed and began reading The Not So Short Introduction To LaTeX 2_ε to learn this typesetting system. All the text currently written will be translated into LaTeX.

Week 38

Completed the LaTeX course. Extended and simulated the PSIM model with a suddenly increasing and decreasing load and observed the transiënt behavior, which was acting as one would expect. From the meeting there became clear that the high-frequency part of the model must be extended with a resonant drive circuit. A paper was found and read about this topic which was very helpful in understanding this extension [7]. Worked at the report and made a planning.

APPENDIX A. TIME TABLE

Week 39

Worked at the report. I'm busy documenting the results found so far in this new -not always simple- LaTeX (especially working with figures!). Found some more interesting documents about resonant MOSFET gate driving [10] [4]. Made a model of a resonant drive circuit and simulated it. I examined the behavior; there is some transiënt time needed to become in steady state. In steady state, this model behaves as expected! I made a print of the model and its behavior and took it to the meeting for comments. From the meeting there became clear that the model needs some extensions. After adding and simulating, the behavior of the model indeed improved.

Week 40

Worked at the report. Made the bibliography correct. Included some index terms. Made a block diagram of the complete power supply. We decided to build our own self oscillating hybrid inverter, with [3] as a starting point. Therefore, I did some readings, calculations and simulations of transformators to refresh my memory. Did some measurements of a toroidal core with one primary and two secondary windings. After that, we measured the inductances, resistances and coupling factors. I also got myself a new handy book to read more about transformers [5]. We found some interesting stuff in here, for instance, the way we can measure the mutual inductance between two sides of the transformer. I bought some components and built a self oscillating hybrid inverter. We did not get this inverter starting up yet. Therefore, we first will try to simulate this circuit.

Week 41

Got the simulation model working of the example in [3]. Worked at the reportings. This is the starting point of our circuit to be build. Made a model of our inverter to be build. Calculated the values needed. I made a simulation and the model seems to work. Went to the lab to get the closest values of the calculated and simulated electrical components. There were some inductors to be wound. I collected all items needed and measured the exact value with the impedance analyzer. Then, I simulated again with the exact found values. With this values, the simulation circuit works. The circuit was made but unfortunately, it didn't work. There must be some problem here.

Week 43

Again tried to get the circuit working, but, without success. I contacted Jorge Duarte for help. While waiting for Jorge's reply, I worked at the report. Jorge gave some hints which indeed worked in a simulation. I now have some clues to get the circuit working, but due to time constrains, I decided first to work at the report, until I'm back at the (last) point of building our own circuit, otherwise, there maybe will be too much time wasted.

Week 44

Worked at the report.

Week 45

Worked at the report. Found some errors in previous calculations, so some of the simulations must be done again. Also, some of the calculations aren't valid anymore. So busy with correcting the report.

Week 46

Worked at the report. Discovered another, better way to control the switch duty ratio of the buck converter. I read about it and calculated, simulated and reported it.

Week 47

Worked at the report. After a meeting with my supervisors, we decided not to report the findings about the resonant drive and the building of our own self-oscillating hybrid inverter due to the current size of the report (¿30 pages).

Week 48

Worked at the report. I tried to finish the report to bring it in to my supervisors, but due to the fact that my help was very hard needed with preparing an exercise for the students of the 5kk70 course and after discussing this with my supervisors, I postponed this event.

Week 51

Worked at the report to finish it before the end of this year. Neatened some slovenly work.

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